

A SiGe Active Sub-Harmonic Front-End for 5-6 GHz Direct-Conversion Receiver Applications

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Abstract — This paper describes the design and measurement of a fabricated SiGe RF front-end for use in direct-conversion receivers for the Unlicensed National Information Infrastructure (U-NII) bands. The front-end is composed of an LNA, I and Q x2 sub-harmonic mixers (SHMs), and an LO conditioning chain. The receiver is completely differential and is designed for operation from a 3.3 V supply. The current consumption is ~6 mA for the LNA and ~5 mA for each mixer. The I/Q mixer pair alone (front-end without LNA) demonstrates ~8-10 dB gain and an IIP2 of ~-29 dBm in the lower U-NII bands. Measured receiver performance (with LNA) shows 18-20 dB conversion gain in the lower two U-NII bands, -16 dBm input compression point, and > 10 dB return loss across all three U-NII bands.

I. INTRODUCTION

There has been considerable recent interest in direct-conversion and low-IF receiver architectures for wireless communication applications. By eliminating the need for expensive, off-chip image reject and band select filters, and allowing amplification and filtering of the down-converted signal to occur at baseband, direct-conversion offers a potentially low-cost, low-power, and highly integrated alternative to the established super-heterodyne receiver [1]-[3].

The concept of direct-conversion is straightforward; however the same is not necessarily true for specific circuit implementations. The translation of the desired RF spectrum to zero-IF dictates that the down-conversion be done in quadrature to recover the “negative-frequency” portion of the spectrum [4]. This adds an additional level of complexity to the receiver. Direct-conversion receivers are also susceptible to dynamic range limitations that further complicate the design, primarily resulting from second-order distortion, 1/f noise, and LO self-mixing. DC-offsets resulting from either nearby interferers or LO leakage self-mixing can also limit the performance of direct-conversion receivers. Sub-harmonic mixing, specifically, can potentially mitigate LO self-mixing, reducing DC-offset problems [5].

This paper presents measured results for a sub-harmonic direct-conversion RFIC front-end designed for 5-6 GHz (U-NII band) applications. A detailed discussion of the design can be found in [6], [7]. The receiver front-end

includes two sub-harmonic mixers for quadrature (I and Q) down-conversion, a differential cascode LNA, and conditioning circuitry to provide the required LO phases to the two mixers. The receiver chip is packaged in a low-profile MLF package, and bondwire and package parasitics are accounted for in the design. The circuit is designed for a supply voltage of 3.3 V. A block diagram of the receiver is shown in Fig. 1.

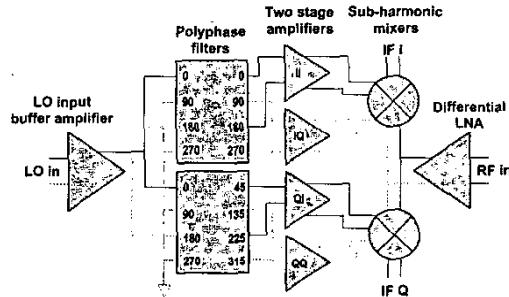


Fig. 1. Block diagram of the receiver front-end.

II. RECEIVER TOPOLOGY AND DESIGN

Fig. 2 shows a simplified schematic for the x2 sub-harmonic mixer. As described in [5], [6], the design and operation of this circuit is based on a stacked Gilbert-cell topology. By applying quadrature LO signals to the mixer switching core, second harmonic mixing can be obtained. Analogous to an exclusive-OR gate, the switching core operates on the applied quadrature signals such that the effective LO presented to the RF input current is at twice the actual LO frequency. Since the circuit is completely differential, not only are the 0° and 90° phases necessary, but also their compliments at 180° and 270° (denoted as the ‘I’ phases). A second sub-harmonic mixer is necessary to attain quadrature RF-to-baseband down-conversion; thus another set of quadrature differential LO signals, with phases at 45°, 135°, 225°, and 315° (denoted as the ‘Q’ phases), is required. In total, the LO signal is split into eight different phases. The resulting LO components are referred to here as II, IQ, QI, and QQ (see Fig. 1).

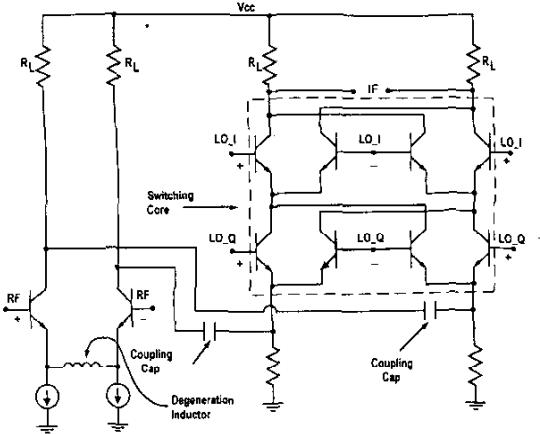


Fig. 2. Schematic of the x2 sub-harmonic mixer core.

The second stage added to the LO switching core would leave significantly less voltage headroom than the standard Gilbert-cell mixer. Therefore, in this design, the RF transconductor is biased in parallel with, and AC coupled to, the LO switching section [6], [7]. Resistors are used to bias this section further reducing voltage requirements.

For evaluation purposes, two other chips containing standalone I and Q sub-harmonic mixer pairs and associated LO conditioning circuits were fabricated. In one case, the LO input to the chip was single-ended (this was also used for the full receiver front-end) to provide a comparison to the prior work in [6]. In the other case, the LO input was fully differential in order to explore the effects of the conditioning circuitry on I and Q phase balance. Simulations show the I/Q phase error is 0° at an LO power of -2 dBm for the differential LO input. All three designs are otherwise identical.

The schematic of the LNA design is shown in Fig. 3. This LNA includes a cascode differential pair for high input/output isolation, with series input inductors for matching, and inductive collector loading to minimize the overall noise figure and to improve voltage headroom. While the LNA input is differential, modifying it to include single-to-differential conversion (e.g. to match to a single-ended band select filter) is straightforward.

Because the receiver is designed for direct-conversion, the need to match to an off-chip image reject filter is eliminated and the impedance between the LNA and the mixers can be set to optimize performance. The same is true for low-IF applications as image rejection can take place at baseband.

The LNA output (RF_{out} in Fig. 3) is directly matched to the input of the I and Q mixers ($RF+$ and $RF-$ in Fig. 2). The two mixers are in parallel, reducing the differential impedance presented to the LNA. Each mixer input match is controlled by emitter inductive degeneration;

increasing the degeneration improves mixer linearity. However, parasitics associated with on-chip inductors limit the amount of inductance that can be used, hence the achievable linearity. For reasonable linearity, a 200Ω differential input impedance for each mixer was chosen, corresponding to a 2.1 nH inductor in each mixer emitter. A simple inter-stage matching network that incorporates the inductive loading of the LNA is used to match the effective 100Ω differential input of the two mixers in parallel to the output of the LNA.

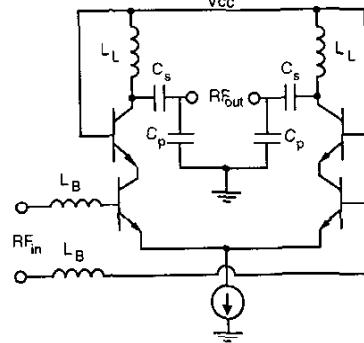


Fig. 3. Simplified schematic of the differential LNA.

III. FABRICATION AND PACKAGING

The chips were fabricated in the IBM 5HP SiGe $0.5\ \mu\text{m}$ BiCMOS process. Fig. 4 shows the layout of the fabricated chip. The differential RF is applied at the right side of the chip, the single-ended LO at the left, and the differential IFs (I & Q) are taken from the top and bottom as indicated. "Guard rings," consisting of rows of substrate contacts placed between deep-trench, are used to enhance isolation between the various sub-circuits, with particular attention to separating the RF/LO sections and the I/Q sections. The LO conditioning circuitry is carefully laid out in order to avoid the detrimental effects of parasitics on the phase balance. This entails "wrapping" the signal carrying lines at fixed distances to make sure the parasitics between lines are identical.

The chip is packaged in a low-profile MLF 32-pin $5\text{ mm} \times 5\text{ mm}$ package. The bond wires and package parasitics were modeled using EM simulations, and accounted for in the front-end RF design. Notably, the bond wire inductance can be beneficial by reducing the total on-chip inductance used for input matching. Fig. 5 shows the fabricated and packaged direct-conversion receiver. The chip is mounted on a custom test board for the measurements.

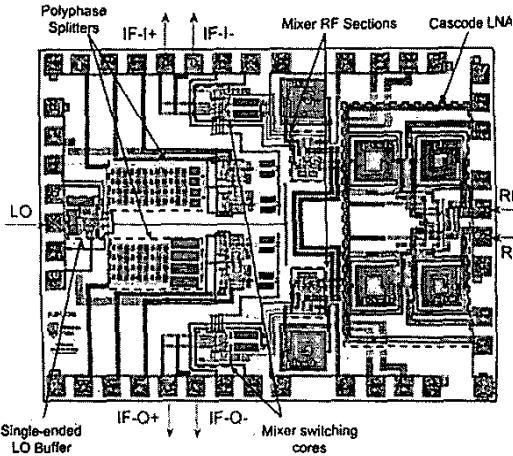


Fig. 4. Detailed layout of the receiver front-end.

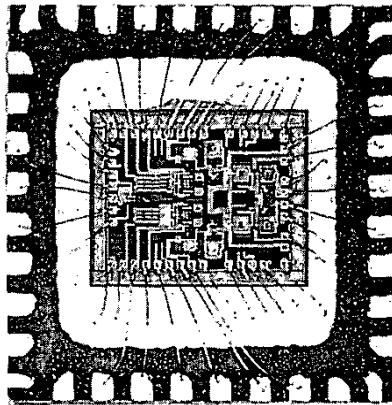


Fig. 5. Photograph of fabricated receiver front-end packaged in 32 pin MLF package. The chip area is 2.3 mm x 1.8 mm.

IV. MEASURED RESULTS

Fig. 6 shows the measured conversion gain of the receiver front-end (single-ended LO) with and without the cascode LNA as a function of RF frequency at an LO power of -5 dBm and an IF of 50 MHz. The measured conversion gain vs. frequency for the receiver (with LNA) is $19 \text{ dB} \pm 1 \text{ dB}$ for the lower two U-NII bands. The gain of the LNA can be inferred from the difference between the solid- and dashed-line curves. Measured results are referenced to the differential $3 \text{ k}\Omega$ output impedance of the mixers.

The measured noise figure of the I and Q standalone mixers is presented in Fig. 7. Over the lower two U-NII bands, the noise figure is between 11 and 12 dB. With the low-noise amplifier cascaded before the mixers, a reduction in the overall noise figure is expected. Simulated results show an overall noise figure for the receiver (with

LNA) of 6.8 dB . Receiver noise figure measurements are currently in progress. The standalone mixers demonstrate >55 dB of $2\text{LO} \rightarrow \text{RF}$ isolation (Fig. 8) and >50 dB of $\text{LO} \rightarrow \text{RF}$ isolation across all three U-NII bands with an LO power of -5 dBm. Isolation should improve with LNA reverse isolation.

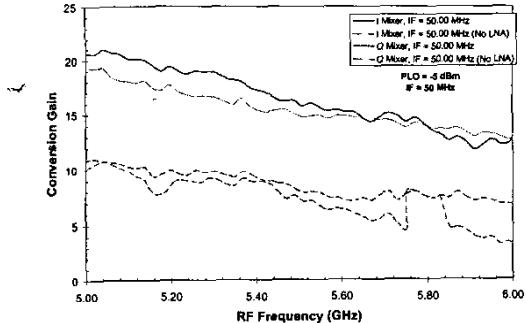


Fig. 6. Measured conversion gain vs. RF frequency of the I and Q channels ($\text{RF} \rightarrow \text{IF-I} \& \text{IF-Q}$) with and without the cascode LNA. Here, the LO is set to -5 dBm and the IF is set to 50 MHz.

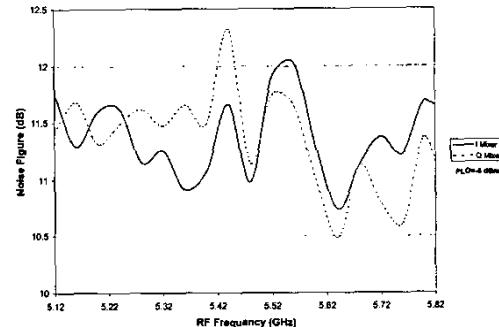


Fig. 7. Measured noise figure of I & Q mixers with the LO set to -5 dBm and the IF set to 50 MHz.

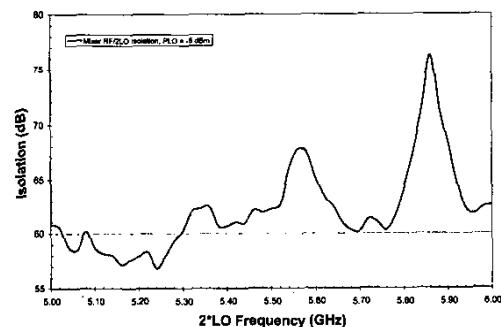


Fig. 8. Measured $2\text{LO} \rightarrow \text{RF}$ isolation of I/Q mixers with LO power set to -5 dBm.

In measuring return loss, the RF signal input is converted from single-ended to differential using a 180° hybrid. The measured VSWR is better than 2:1 (10 dB return loss) over each of the three U-NII bands. At an RF of 5.2 GHz and an IF of 50 MHz, the input 1dB compression point is measured to be -16 dBm. The current consumption is ~ 6 mA for the LNA and ~ 5 mA for each mixer.

The second order intercept point (IP2) can serve as a reasonable measure of second order non-linearities in a receiver [1]. This is important for direct-conversion or low-IF receiver architectures as second order products will appear in-band and may degrade receiver performance. Second order non-linearities can be reduced significantly by using balanced or differential circuitry. In the case of the two chips with single-to-differential LO input buffers, perfect balance was not achieved and the IIP2 was considerably degraded. However, using a differential LO input, the IIP2 is improved. Fig. 8 shows the IIP2 of the standalone mixers with a differential LO input. With the two RF tones set to 5.246 GHz and 5.254 GHz, and an IF of 50 MHz, the IIP2 is measured to be $+29$ dBm.

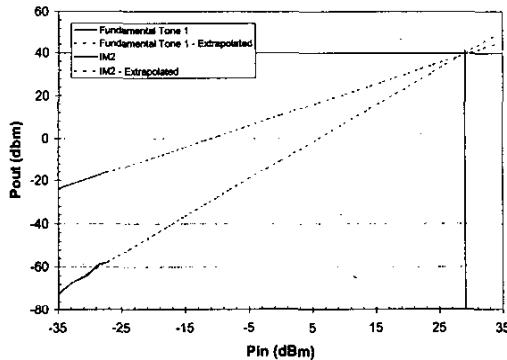


Fig. 9. Input IP2 of standalone mixers with LO signal applied via a differential buffer. RF1 = 5.246 GHz, RF2 = 5.254 GHz, IF = 50 MHz.

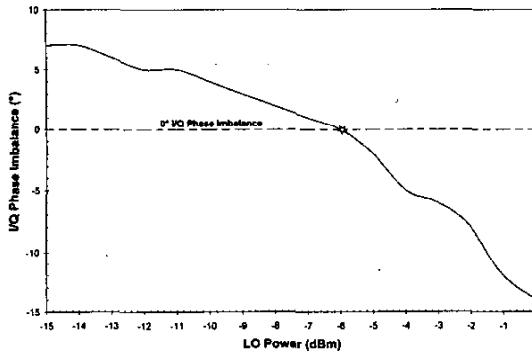


Fig. 10. Measured I/Q phase imbalance vs. LO power with an IF of 50 MHz. 0° phase error is achieved at -6 dBm LO power.

Fig. 10 shows the measured I/Q phase imbalance for the standalone mixers with a differential LO input. At an LO power of -6 dBm, the imbalance between I and Q is exactly 0° .

V. CONCLUSION

The paper describes the design and implementation of an *active sub-harmonic* direct conversion receiver in SiGe for 5-6 GHz applications. Measured receiver performance (with LNA) shows 18-20 dB conversion gain in the lower two U-NII bands, -16 dBm input compression point, and > 10 dB return loss across all three U-NII bands. Using fully differential LO conditioning circuitry, the IIP2 of the sub-harmonic mixers is measured to be $+29$ dBm while an I/Q phase imbalance of exactly 0° is achieved. The performance results presented here meet the requirements cited in [2] for WLAN products. Further characterization, such as receiver noise figure, is in progress.

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